DETAILED ACTION

1. This communication is responsive to Amendment filed 11/13/2007.

2. Claims 1-96 are pending in this application. Claims 7 and 37 are independent claims. In Amendment, claims 1-6, 8-10, 15-18, 21, 26-28, 38, 41-45, 54-69, 71-73, 78-81 and 83-96 are previously withdrawn from the consideration. This Office Action is made non-final after considering Pre-Brief Conference request dated 11/13/2007.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 7, 11-14, 19-20, 22-25, 29-37, 39-42, 46-53, 70, 74-77 and 82 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claim 7, the limitation "free bit in a register" is not clearly defined in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In addition, the applicant fails to provide a clear definition of free bit (e.g. as value 0/1) within the

register nor the support for the clear definition in the original specification for examination purposes. Claims 20 and 37 have the same rejection.

Thus, claims 11-14, 19, 22-25, 29-36, 39-42, 46-53, 70, 74-77 and 82 are also rejected for being dependent on the rejected base claims 7, 20, and 37.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7, 11-14, 19-20, 22-25, 29-37, 39-42, 46-53, 70, 74-77 and 82 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 7, the limitation "free bit" is unclear since it does not clearly define what is the free bit as whether the free bit is false bit as 0 or the free bit is true bit as 1. For examination purposes, the examiner considers the free bit in the claim means false bit as 0. In addition, it is unclear how to select the available part know which part has the free bit in order to select the part. Thus, the claim is also rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the step to determining which part of the parts of the available parts that has the free bit. Claims 20 and 37 have similar rejection as cited in claim 7. Further, most of the claims do not have structural between features/limitations within the claims.

Re claim 20, it is unclear whether this claim is an apparatus claim or a method claim since it is a hybrid claim. For examination purposes, the examiner considers this

claim as an apparatus claim having a first breaker and a selector as cited in the claim. Claim 37 has the similar rejection as cited in claim 20. In addition, claim 70, 74-77 and 82 have similar rejection as cited in claim 20 for the computer software product.

Thus, claims 11-14, 19, 22-25, 29-36, 39-42 and 46-53 are also rejected for being dependent on the rejected base claims 7, 20, and 37.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 20, 22-25, 29-37, 39-42, 46-53, 70, 74-77 and 82 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 20, 22-25, 29-37, 39-42, 46-53, 70, 74-77, and 82 cite a method, apparatus, and software product for performing an operation. However, claims 20, 22-25, 29-37, 39-42, and 46-53 merely disclose series of mental steps for performing the operation without disclosing a practical/physical application or a useful and tangible result in real world application. The claims 20, 22-25, 29-37, 39-42, and 46-53 appear to preempt every substantial practical application of the idea embodied by the claims. Further, these claims are considered as software per se since the means can be software module. In addition, claims 70, 74-77 and 82 are considered as non-functional program code since they do not include a tangible medium and being executed by the computer to carry the intended operation. Therefore, claims 20, 22-25, 29-37, 39-42, 46-53, 70, 74-77, and 82 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

10. Claims 7, 11, 13, 20, 22-24, 29-31, 33, 36-37, 39-41, 46-48, 50, 53, 70, 74, and 76 are rejected under 35 U.S.C. 102(a) as being anticipated by Ott (U.S. 6,477,552).

Re claim 7, Ott discloses in Figures 1-4 a method for finding a next free bit in a register having N bits and a current pointer pointing to one of the bits (e.g. abstract wherein the free bit is the zero bit within the nibble and N is equated to 32 bits in the source register rs1 as seen in Figures 1-2), the method comprising:

breaking the N bits of a check vector in the register into M parts, wherein N and M are integers and 1<M<N (e.g. Figure 2 wherein 32-bits of source register rs1 are break down into 8 parts and each part consists of 4 bits as nibble to corresponding nibble logics 22x); and

selecting an available part that has a free bit (e.g. output of the priority encoder in Figure 2 for selecting the part of 0 bit and col. 3 lines 1-25).

Re claim 11, Ott further discloses in Figures 1-4 the available part is a first part, having a free bit, to the left of the part pointed to by the current pointer (e.g. Figure 4 table).

Re claim 13, Ott further discloses in Figures 1-4 finding a free bit in the available part (e.g. abstract).

Re claim 20, it is an apparatus claim of claim 7. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 22, it is an apparatus claim of claim 11. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 23, Ott further discloses in Figures 1-4 a check sector generator for generating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts (e.g. Figure 2).

Re claim 24, Ott further discloses in Figures 1-4 a second breaker for breaking the current pointer into upper bits and lower bits, wherein the current pointer has X bits, the upper bits have Y bits and a value U, and the lower bits have X-Y bits and a value L, and wherein 0 <=U<=e^y-1, and 0<=L<=2^(x-y)-l, where all of X, Y, U, and L are integers (e.g. Figures 1-2).

Re claim 29, it has similar limitations cited in claim 13. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 30, it has similar limitations cited in claim 11. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 31, it has similar limitations cited in claim 24. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 33, Ott further discloses in Figures 1-4 the free bit finder finds a free bit from the beginning of the available part (e.g. Figure 4 table).

Re claim 36, Ott further discloses in Figures 1-4 a next vector generator for generating the next vector with the found free bit masked (e.g. output of Figure 2).

Re claim 37, it is a means apparatus claim of claim 20. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 20.

Re claim 39, it is a means apparatus claim of claim 22. Thus, claim 39 is also rejected under the same rationale as cited in the rejection of rejected claim 22.

Re claim 40, it is a means apparatus claim of claim 23. Thus, claim 40 is also rejected under the same rationale as cited in the rejection of rejected claim 23.

Re claim 41, it is a means apparatus claim of claim 24. Thus, claim 41 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 46, it is a means apparatus claim of claim 29. Thus, claim 46 is also rejected under the same rationale as cited in the rejection of rejected claim 29.

Re claim 47, it is a means apparatus claim of claim 30. Thus, claim 47 is also rejected under the same rationale as cited in the rejection of rejected claim 30.

Re claim 48, it is a means apparatus claim of claim 31. Thus, claim 48 is also rejected under the same rationale as cited in the rejection of rejected claim 31.

Re claim 50, it is a means apparatus claim of claim 33. Thus, claim 50 is also rejected under the same rationale as cited in the rejection of rejected claim 33.

Re claim 53, it is a means apparatus claim of claim 36. Thus, claim 53 is also rejected under the same rationale as cited in the rejection of rejected claim 36.

Re claim 70, it is a computer software product claim of claim 7. Thus, claim 70 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 74, it is a computer software product claim of claim 11. Thus, claim 74 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 76, it is a computer software product claim of claim 13. Thus, claim 76 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Response to Arguments

11. Applicant's arguments with respect to claims 7, 11-14, 19-20, 22-25, 29-37, 39-42, 46-53, 70, 74-77 and 82 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Chat C. Do/
Primary Examiner, Art Unit 2193

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